REMARKS

At the outset, Applicant wishes to thank the Examiner for the courtesies extended to the Applicants' representatives during the personal interview on April 12, 2004. The final Office Action of January 27, 2004 has been received and contents carefully reviewed.

By this Amendment, Applicant amends claims 82-84, and adds new claims 85-88. In addition, Applicant cancels claims 38-55 without disclaimer or prejudice. Accordingly, claims 27-37 and 56-88 are currently pending in the present application. Reexamination and reconsideration of the application are respectfully requested.

In the Office Action, the Examiner rejected 82-84 under 35 U.S.C. § 102(e) as being anticipated by Yasui et al. (U.S. Patent No. 5,784,039); claims 27-33, 36-46, 49-63 and 65-81 under 35 U.S.C. § 103(a) as being unpatentable over Yasui et al. in view of Kubota et al. (U.S. Patent No. 5,754,155); rejected claims 35 and 48 under 35 U.S.C. § 103(a) as being unpatentable over Yasui et al. in view of Kubota et al., and further in view of Applicant's Prior Art (APA); rejected claims 34, 47 and 64 under 35 U.S.C. § 103(a) as being unpatentable over Yasui et al. in view of Kubota et al., and further in view of Hirai et al. (U.S. Patent No. 5,646,643). These rejections are respectfully traversed and reconsideration is requested.

Claim 27 is allowable over the cited references in that claim 27 recites a combination of elements including, for example, "wherein the gate controller applies gate control signals that cause the gate driver to apply the second voltage to the gate signal line after the application of the first signal voltage, but during the application of the data signal to the pixel electrode through the data signal line ..." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 27 and claims 28-37, which depend therefrom, are allowable over the cited references.

In the Office Action on page 10, the Examiner states with respect to claim 27, "the gate controller 3 applies gate control signal that cause the gate driver 3 to apply the second voltage V_{GL} to the gate signal line Gi after the application of the first signal voltage V_{GH}, but *during the application of the data signal (V_S) to the pixel electrode (C_{LC}) through the data signal line (S)* (see figures 1A and 3B)." However, Applicant respectfully submits that Yasui et al. does not

disclose such a feature, as it can be seen from Fig. 3B in which the TFT is turned off during the period between t1 and t2. See Fig. 3B of Yasui et al.

Claim 56 is allowable over the cited references in that claim 56 recites a combination of elements including, for example, "said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transitioning to the second gate voltage, wherein the second gate voltage has a voltage level that turns off the switching transistor." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 56, and claims 57-61 and 65-70 which depend therefrom, are allowable over the cited references.

In the Office Action on page 7, the Examiner states, "...the first gate voltage V_{sat} + $V_{on(PIX)}$ reducing a voltage level substantially to a threshold voltage level $V_{th(PIX)}$... (see figure 2, column 9, lines 20-30)." The Examiner further states on the same page, "It would have been obvious... to utilize $V_{GH'} > V_{sat} + V_{on(PIX)}$ by only $V_{th(PIX)}$... because this would display an image with high quality and excellent "

First of all, the switching transistor in claim 56 refers to a pixel transistor. However, $V_{th(PIX)}$ in Kubota et al. is a threshold voltage of the $TR_{(PIX)}$, which is a transistor used in the reference voltage generating circuit and has the approximately same threshold voltage as the picture element transistors. See Fig. 2 and Col. 10, lines 47-61 of Kubota et al. Secondly, Applicant respectfully submits that, as best understood, the formula "$V_{GH'} > V_{sat} + V_{on(PIX)}$ by only $V_{th(PIX)}$" in Kubota et al. means $V_{GH'} = V_{sat} + V_{on(PIX)} + V_{th(PIX)}$. In other words, $V_{GH'}$ is higher than $V_{th(PIX)}$ by $V_{sat} + V_{on(PIX)}$, which thus does not teach or suggest the feature, "said first gate voltage reducing a voltage level substantially to a threshold voltage level... of the switching transistor" as claimed in claim 56.

Claim 62 is allowable over the cited references in that claim 62 recites a combination of elements including, for example, "supplying the first gate voltage and the second gate voltage selectively via a switching device, to the gate lines, said switching device being controlled by the shift register, said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transitioning to the second gate voltage." None of the cited references, singly or in combination, teaches or suggests

at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 62 and claims 63-64 which depend therefrom, are allowable over the cited references.

Claim 71 is allowable over the cited references in that claim 71 recites a combination of elements including, for example, "a gate driver connected to the plurality of scanning signal lines, said gate driver receiving first and second control voltages and a scanning clock signal and, in response to the scanning clock signal, successively outputting the first control voltage to the scanning signal lines to drive the scanning signal lines, wherein the switching device of each pixel responds to the first control voltage to connect the first electrode with the pixel electrode, and responds to the second control voltage to disconnect the first electrode from the pixel electrode, wherein a voltage level of the first control voltage received by the gate driver changes during a period of the scanning clock signal prior to the driver selecting a successive scanning line, and wherein the voltage level of the first control voltage turns on the switching device and the voltage level of the first control voltage is reduced substantially to a threshold voltage level but enough to maintain an on-state of the switching device during the period of the scanning clock signal prior to the driver selecting the successive scanning line." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 71, and claims 72-75 which depend therefrom, are allowable over the cited references.

Claim 76 is allowable over the cited references in that claim 76 recites a combination of elements including, for example, "sequentially applying a first voltage to each of the plurality of scanning lines, wherein the first voltage electrically connects the plurality of contact electrodes to the plurality of pixel electrodes; and sequentially applying a second voltage to each of the plurality of scanning lines, wherein the second voltage electrically disconnects the plurality of contact electrodes from the plurality of pixel electrodes, wherein the second voltage is sequentially applied to each of the plurality of scanning lines after the application of the first voltage to each of the plurality of scanning lines but prior to the sequential application of the first voltage to another one of the plurality of scanning lines." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 76, and claims 77-81 which depend therefrom, are allowable over the cited references.

Claim 82 is allowable over the cited references in that claim 82 recites a combination of elements including, for example, "high level and low level voltage generators electrically connected to the gate driver and outputting the first and second voltage levels to the gate driver, respectively, the high level voltage generator including a means for changing a falling edge of the scanning signal ..." Accordingly, Applicant respectfully submits that claim 82 and claims 83-88 which depend therefrom, are allowable over the cited references.

Applicant believes the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number (202) 496 – 7500. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

Dated: April 26, 2004

Respectfully submitted,

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